Xenomai: Real-Time Framework for Linux

http://xenomai.org/



Xenomai on NIOS II Softcore Processor: a step by step Guide

Author:P. Kadionik and Ph. GerumVersion:1.2Date:04/01/2010

Patrice Kadionik: kadionik@enseirb-matmeca.fr Philippe Gerum: rpm@xenomai.org

TABLE OF CONTENTS

1.Introduction	4
2. The Altera NIOS II softcore processor	5
3.Hardware configuration: a step by step guide	9
3.1.The target board used as an example	9
3.2.Building the SoPC system	10
4.Software configuration: a step by step guide	23
4.1.Altera tool installation under Linux	23
4.2.Linux configuration for the NIOS II processor	24
4.3.Xenomai configuration for the NIOS II processor	28
5.References	31

Summary

Hard	lware
Target processor	NIOS II
Vendor	Altera
Synthesis tools	Quartus II version 9.0 at least
Target board example	Altera Stratix 1S10
Software versions	s used in this guide
Linux distribution	Fedora 12
Linux version for NIOS II	μClinux 2.6.30
Cross compiler for NIOS II	3.4.6
<i>ipipe</i> patch version for NIOS II	adeos-ipipe-2.6.30-nios2-1.1-00.patch
Xenomai version	2.5.2

Document version:

Date	Version	Comments
11/16/2009	1.0	Initial version
01/10/2010	1.1	Updated to Xenomai 2.5.0. Text corrections
04/01/2010	1.2	Updated to Xenomai 2.5.2. Text corrections. Adding design rule on timer
		creation

1. INTRODUCTION

This guide explains how to set-up your SoPC (*System on Programmable Chip*) design for running Xenomai. Altera's Stratix 1S10 board is the reference target throughout the document. However, the contents of this guide should be applicable to similar hardware as well.

2. THE ALTERA NIOS II SOFTCORE PROCESSOR

The NIOS II processor (second generation of the NIOS processor) is a RISC softcore processor with a Harvard architecture. It has up to 6 pipeline stages and has a 32-bit data bus.



Figure 1: NIOS II processor architecture

The following table resumes its main characteristics:

	NIOS II Processor
	RISC architecture
	32-bit instructions
•	32 32-bit general registers
	32 IRQs
	Instruction and data caches
-	Custom instructions

Figure 2: Main characteristics of the NIOS II processor

During the configuration of the NIOS II processor with the *SOPC Builder* tool, you can choose between three versions for the processor:

- The *Economy* version that uses less silicon area on the FPGA circuit.
- The *Standard* version that allows a good compromise between area and speed.
- The *Fast* version is the fastest (in frequency) version.

	NIOS II /f	NIOS II /s	NIOS II /e
Pipeline	6 levels	5 levels	No
HW Multiplication	1 Cycle	3 Cycles	By SW
Branch Prediction	Dynamic	Static	No
Instruction Cache	Configurable	Configurable	No
Data Cache	Configurable	No	No
Custom Instructions		Up to 256	

Figure 3: The different versions of the NIOS II processor

The following figure shows the performances in DMIPS (*Dhrystone Million Instructions per Second*) and the used area in Altera Logic Elements for different versions of the NIOS II processor on different families of Altera FPGA circuits (Stratix, Stratix II, Cyclone, Cyclone II ...).



Figure 4: NIOS II processor performances

When you build your SoPC system with the *SOPC Builder* tool, it is possible to include various devices using the Altera Avalon bus:

- Memory.
- Timer.
- UART serial line.
- LCD screen.
- GPIO.
- Ethernet interface.
- CompactFlash interface.
- JTAG.
- ...



Figure 5: Altera Avalon bus

3. HARDWARE CONFIGURATION: A STEP BY STEP GUIDE

3.1. The target board used as an example

For this tutorial, we have chosen a development board from Altera: the Stratix 1S10 board.



Figure 6: Altera Stratix 1S10 target board

The Stratix 1S10 board has the following features:

- A Stratix EP1S10F780C6 device.
- 8 Mbytes of flash memory.
- 1 Mbyte of static RAM.
- 16 Mbytes of SDRAM.
- On board logic for configuring the Stratix device from flash memory.
- On-board Ethernet MAC/PHY device.
- Two 5-V-tolerant expansion/prototype headers each with access to 41 Stratix user I/O pins.
- CompactFlash connector header for Type I CompactFlash (CF) cards.
- Mictor connector for hardware and software debug.
- Two RS-232 DB9 serial ports.
- Four push-button switches connected to Stratix user I/O pins.
- Eight leds connected to Stratix user I/O pins.

- Dual 7-segment LED display.
- JTAG connectors to Altera devices via Altera download cables.
- 50 MHz oscillator and zero-skew clock distribution circuitry.
- Power-on reset circuitry.

3.2. Building the SoPC system

You have to use the Altera *Quartus II* tool for building the SoPC system compatible with the Xenomai port. The FPGA synthesis process builds a *.sof* file, which will be usable in turn for programming the FPGA circuit on the target board with the JTAG module.

1. Reference design

The *Quartus II* reference design for embedded Linux with or without real-time extension has been built from the *standard* reference design provided by Altera for the Stratix 1S10 board.

This *standard* reference design is generally provided for all Altera boards and is a good start for using Embedded Linux.

The following figure shows the *standard* reference design for the Stratix 1S10 target board:



Figure 7: standard reference design for the Altera Stratix 1S10 target board

Modify this reference design with the SoPC Builder tool.

The three following figures show the new SoPC configuration. New timers have been introduced in the design for compatibility with the Xenomai port for the NIOS II processor.

Component Library	Target			CIUCK SE	un igs					_	
 Nios Il Processor 	Device	Family: Strati	×	Name	•	Source		M	Hz		Ad
-Bridges and Adapters -Interface Protocols				clk sys_c	lk	External pll.c0		50, 50,	0 D	Re	mo
-Legacy Components -Memories and Memory Control -Perinherals				sdran	n cik out	pll.e0		150.1	0		
Debug and Performance	Use	Connec	Module Name		Description		Clock	IRQ	Base	End	
-Display -FPGA Peripherals -Microcontroller Peripherals -Microcontroller Veripherals -Microcontroller Veripherals			cpu instruction_m data_master itag debug r	naster nodule	Nios II Processor Avalon Memory M Avalon Memory M Avalon Memory M	apped Master apped Master apped Slave	sys_cik	5	IRQ 0	IRQ 0x008107ff	3:
PIO (Parallel I/O) Multiprocessor Coordinatic PLL UCP			ext_ram_bus avalon_slave tristate_mast	er	Avalon-MM Tristal Avalon Memory M Avalon Memory M	e Bridge apped Slave apped Tristate Master	sys_cik				
·Usb ·Video and Image Processing		$ \mapsto$	E ext_flash s1 E ext_ram		Flash Memory Inte Avalon Memory M	rface (CFI) apped Tristate Slave	sys_cik		≝ 0 ∞0000000	0x007fffff	
			s1	64 kbat	Avalon Memory M	apped Tristate Slave	aya_uk		⊪ 0 ∞02000000	0x020fffff	
		$ \searrow \rightarrow$	s1	<u>.04_RD</u> ytaa	Avalon Memory M	apped Slave	sys_clk		≝ 0x02100000	0x0210ffff	
•		$ \rightarrow$	s1		Avalon Memory M	apped Slave	sys_clk	一前	■ 0x00810860	0x0081087f	
		$ \rightarrow$	🕀 hrclock		Interval Timer		sys_clk		· 0x00810900	0x0081093f	
Edit Add	Remo	ve Edit	hrtimer s1 hrclock		Interval Timer Avalon Memory M Interval Timer	apped Slave	sys_clk sys_clk	efault	0x00810860	0x0081087f 0x0081093f	

	Target			CIUCK SE	aungs						
Component Library	Device	Family Strat	tix 🖃								0 dd
Nios Il Processor Reidges and Adortors	2.511001	unity (Our di		Name	•	Source		M	Hz.		Mad
I-bridges and Adapters				CIK	lk	External		50,0	,	F	temov
-Legacy Components				sdran	n clk out	pli.e0		50.0)	*	
Memories and Memory Control											
Peripherals		_	1		1				-	1	
Debug and Performance Display	Use	Connec	Module Name		Description		Clock	IRQ	Base	End	
FPGA Peripherals					Avalop Memory Ma	aned Slave	eve clk	L h	- 0-0081086	0 0v0081087f	
Microcontroller Peripherals		$ \rangle \rightarrow$	E hrclock		Interval Timer		sys_clk	2	· 0x0081090	0 0x0081093f	
Interval Timer Dio (Perelle 1/0)			sys_clk_time	er	Interval Timer		2010	I			
Multiprocessor Coordinatic		$ \rightarrow$	⇒ s1		Avalon Memory Ma	oped Slave	sys_cik	≻-þ	0x0081080	0 0x0081081f	
9-PLL			avalon itag	slave	Avalon Memory Ma	aned Slave	svs clk	لملح ا	0x0081082	0×00810827	
USB			⊡ uart1		UART (RS-232 Seri	al Port)	-9-2	Ϊ			
-Video and Image Processing		$ \rightarrow$	⇒ s1		Avalon Memory Ma	oped Slave	sys_cik	≻−₽	- 0x0081084	0 0x0081085f	
			□ button_pio		PIO (Parallel I/O)	aned Sleve	ove alk				
			E led pio		PIO (Parallel I/O)	opeu siave	sys_cik	Í	= 0x0061083	0 0x00810831	5
		$ \rightarrow$	→ s1		Avalon Memory Ma	oped Slave	sys_clk		0x0081088	0 0x0081088f	
			E seven_seg_	pio	PIO (Parallel I/O)	and Cr	led_pio.s1				
•		$ \uparrow\uparrow\rangle$	S1	west nic	Avaion Memory Ma PIO (Parallel I/O)	oped Slave	Avalon Mer	nory Mapp	ed Slave [avalon_	slave 9.0] 1089 f	
											•
			Exit Hel	p	Prev Nex	t 🕨 🛛 G	enerate				
Alt Edit Module System View 1 m Contents]System Generation	era SOPC I fools Nios	Quilder - sto Il Help	Exit Hel d_1s10.sopc (D:tr	p mp\design	Prev Nex	t D G	enerate q9.0_v3.0\std_1	s10.sopc)		00
Ait Edit Module System View 1 am Contents System Generation	era SOPC f fools Nios Target	Builder - st II Help	Exit Hel d_1s10.sopc (D:tr	p mp\design	Prev Nex	t D G	enerate q9.0_v3.0\std_1	s10.sopc)		0
Alt Edit Module System View 1 mr Contents System Generation Component Library — Nics II Processor	rera SOPC I Fools Nios Target Device I	Builder - st II Help Family; Strat	Exit Hel d_1s10.sopc (D:tr tix *	p mp\design 	Prev Nex r_xenomal_v3:stan tlings	t D G	enerate q9.0_v3.0\std_1	Is10.sopc) 4z		Add
Alt Edit Module System View 1 m Contents System Generation Component Library — • Nios Il Processor Bridges and Adapters	Target	Builder - st II Help Family: Strat	Ext Hel d_1s10.sope (D:tr	p mp\design Clock Se Name clk	Prev Nex Income second s	t C dard_Xenomai_ Source External	enerate q9.0_v3.0\std_1	Is10.sopc) 12 0		Add
All Edit Module System View 1 m Contents System Generation Component Library • Nios Il Processor Pridges and Adapters Interface Protocols	Fools Nios Target Device I	fuilder - st II Help Family: Strat	Ext Hel d_1s10.sope (0:tr tix *	P Clock See Clock See Clk Sys_c	Prev Nex Intervention	dard_Xenomai_	enerate	MI 50,(50,0) 1 <u>7</u>		O I
Alt Edit Module System View 1 m Contents System Generation Component Library - Nios II Processor Bridges and Adapters - Interface Protocols - Legacy Components - Legacy Components	Fools Nios	Juilder - st II Help ∓amily: Strat	Ext Hel d_1s10.sopc (D:tr tix *	P Clock Se Clock Se Clk Sys_c Sdran	Prev Nex ttings ttings k k n elk out	dard_Xenomai_ Source External pl.c0 pl.e0	enerate q9.0_v3.0\std_1	MH 50,0 50,0) 1 <u>z</u>)		Add
Alt Edit Module System View 1 m Contents System Generation Component Library Pridges and Adapters - Interface Protocols - Legacy Components - Memories and Memory Control - Peripherals	Fools Nios	builder - st II Help Family: Strat	Ext Hel	P Clock Se Clock Se Clk Sys_c sdran	Prev Nex ttings h k n clk out	dard_Xenomai_ Source External plLe0 plLe0	enerate q9.0_v3.0\std_1	S10.Sopc MI 50,0 50,0 50,0) 4z))		O I
Alt Edit Module System View 1 im Contents System Generation Component Library Nos II Processor Bridges and Adapters Interface Protocols Legacy Components Memories and Memory Control Peripherals	Target Device I	Ruilder - st II Help Family: Strat	Exit Hel d_1s10.sopc (D:tr tix * Module Name	P Clock Ser Clock Ser Clk Sys_C sdran	Prev Nex xenomai_v3'stan ttings k n clk out Description	dard_Xenomai_	g9.0_v3.0\std_1	MI 50,0 50,0 50,0 1RQ) 12))) Base	Ènd	Add Remov
Alt Edit Module System View 1 m Contents System Generation Component Library Nos II Processor Pridges and Adapters Interface Protocols Legacy Components Memory Control Peripherals Debug and Performance Display Store Double performance	Target	Connec	Exit Hel d_1s10.sopc (D:tr tix * Module Name	P Clock Ser Clock Ser Clock Ser Clock Ser Sys_c sdran	Prev Nex rxenomal_v3istan ttings k n clk out Description PIO (Parallel I/O) rverere 0	dard_Xenomai_ Gard_Xenomai_ Source External pll.e0 bil.e0	enerate q9.0_v3.0\std_1 Clock	Mi 50,0 50,0 1RQ) tz)) Base	End	Add
Alt Edit Module System View 1 m Contents System Generation Component Library Nios II Processor Bridges and Adapters Interface Protocols Uegacy Components Memories and Memory Control Peripherals Display Display ProCA Peripherals Microcolar Peripherals Microcolar Peripherals	era SOPC E fools Nios Target Device I Use	tuilder - st II Help Family; Strat	Ext Hel d_1s10.sopc (D:tu tix Module Name Seven_seg_ s1 peopfin per	P Clock Se clk sys_c sdran	Prev Nez rxenomai_v3istan ttings k n cik out Description PIO (Paralel I/O) Avaion Memory Mon PIO (Paralel I/O) PIO	dard_Xenomai_ dard_Xenomai_ Source External pll.c0 pll.e0	enerate g9.0_v3.0\std_1 Clock sys_clk	MI 50,0 50,0 50,0) 12 0) Base 0x0081089	End 0 0x0081089f	Add
Alt Edit Module System View 1 m Contents System Generation Component Library Nois II Processor Bridges and Adapters Interface Protocols Hegacy Components Hemories and Memory Control Peripherals Display PFPGA Peripherals Microcontroller Peripherals Microcontroller Peripherals Microcontroller Peripherals	era SOPC I fools Nios Target Device I Use	Euilder - st II Help Family: Strat	Ext Hel d_1s10.sopc (D:tu tix Module Name seven_seg_ s1 reconfig_rec s1	P Clock Ser Clock Ser Clock Ser Clock Ser Sdran	Prev Nez recenomal_v3istan tings k n clk out Description Pio (Parallel I/O) Avalon Memory Ma Pio (Parallel I/O) Avalon Memory Ma	t C dard Xenomai Source External pll.c0 pll.c0 pll.e0	enerate q9.0_v3.0\std_1 Clock sys_clk sys_clk	Mi 50,(50,0 1RQ	iz)) Base ■ 0×0081089	End 0 0x0081089f 0 0x008108af	Add
Alt Edit Module System View 1 m Contents System Generation Component Library Pridges and Adapters Interrace Protocols Hergocy Components Memories and Memory Control Perpiperals Perpiperals ProCA Peripherals Memorical Peripherals ProCA Peripherals	era SOPC f fools Nios Target Device I Use	Connec	Ext Hel d_1s10.sopc (D:tr tix * Module Name seven_seg_ s1 reconfig_rec s1 sdram	P Clock Ser Clock Ser Clock Ser Sys_c sdran	Prev Nex Kenomai_v3istan ttings It Description PIO (Parallel I/O) Avalon Memory Ma PIO (Parallel I/O) Avalon Memory Ma SORAM Controller	t C dard_Xenomai_ Source External pl.c0 pl.c0 pl.c0 pl.c0 pl.c0 pl.c0 pl.c0	enerate q9.0_v3.0\std_1 Clock sys_clk sys_clk	MH 50,0 50,0 1RQ) 4z)) Base 0x0081089 a ² 0x0081089	End 0 0x008108af	Add
Alt Edit Module System View 1 m Contents System Generation Component Library Nios II Processor Dridges and Adapters Interface Protocols Legacy Components Memories and Memory Control Perpharals Debug and Performance Display FPGA Peripherals Microcontroller Microntroller Microcontroller Microcontroller Mic	Fools Nios Target Device I Use	Connec	Exit Hel d_1s10.sopc (D:tr tix * Module Name = seven_seg_ s1 = sfam s1 :	P Clock Ser Clock Ser Clk Sys Sdran	Prev Nes Incline	dard_Xenomai_ dard_Xenomai_ Source External pll.0 bll.0 bll.0 pll.	enerate q9.0_v3.0\std_1 Clock sys_clk sys_clk sys_clk	MI 50,0 50,0 1RQ) 12 2 3 3 4 5 5 5 5 5 5 5 5 5 5 5 5 5	End 0 0x0081089f 0 0x0081089f 0 0x010fffff	Add
Ait Edit Module System View 1 im Contents System Generation Component Library Nos Il Processor Pridges and Adapters Intertace Protocols Debug and Performance Display FPGA Peripherals Memory Control Peripherals Merocontroller Peripherals Micro Control	Target Device I Use	Connec	Ext Hel d_1s10.sopc (D:tu itx * Module Name Seven_seg_ s1 scored structure systd systd	P Clock Ser Click Sys_c sdran pio	Prev Nez xenomal_v3istan tings b loscription PIO (Parallel I/O) Avaion Memory Ma SDRAM Controller SDRAM Controller SDRAM Controller Avaion Memory Ma System ID Peripher Avaion Memory Ma System ID Peripher	dard Xenomai dard Xenomai Source External pll.e0 pll.e0 pll.e0 pll.e0 pll.e0 pll.e0 pll.e0	enerate	MI 50,0 50,0 1RQ) Hz Base 0x0081089 0x0081083 0x0081084 0x00810 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0081 0x0084 0x0081	End 0 0x0081089f 0 0x008108af 0 0x010fffff 9 0x001026f	Add
All Edit Module System View m Contents System Generation Component Library Nickles and Adapters Interface Protocols Interface Protocols Interface Protocols Interface Protocols Interval Timer Display FPGA Peripherals Microcontroller Peripherals Microcontr	era SOPC I fools Nios Target Device I Use V V	Connec	Ext Hel d_1s10.sopc (D:ta tix Module Name Seven_seg_ s1 reconfig_rec s1 sdram sysid control_slav p bl	e e p p p p p p p p p p p p p p p p p p	Prev Nez Kenomai_v3istan tings Itings Iti	dard Xenomai Source External pli.e0 Dil.e0 Dil.e0 aped Slave aped Slave apped Slave apped Slave	enerate g3.0_v3.0\std_1 Clock sys_clk sys_clk sys_clk sys_clk	MM 50,(,) 50,0 50,0 1RQ	 12 13 14 14 15 16 	End 0 0x0081089f 0 0x0081089f 0 0x01fffff 0 0x01ffffff 8 0x0081082f	Add
Alt Edit Module System View 1 m Contents System Generation Component Library • Nios II Processor Bridges and Adapters • Interface Profocols • Legacy Components • Despia • Despia and Memory Control • Peripherals • Debug and Performance • Dispia • Dispia • PFGA Peripherals • Microcontroller Peripherals • Dispia • Pio (Parallel I/O) • Multprocessor Coordinatic • PLL • USB • Video and Image Processing	era SOPC I fools Nios Target Device I Use V V V	Euilder - st II Help	Exit Hel d_1s10.sopc (D:tr tx	P Clock Se Clock Se Clock Se Clock Se Sdran	Prev Nez trings tings the second secon	dard_Xenomai_ dard_Xenomai_ Source External pil.c0 pil.c0 pil.e0 oped Slave oped Slave oped Slave oped Slave oped Slave	enerate	MM 50,0 50 (160) 4z Base 0x0081083 0x0081083 0x0081082 0x0081082 0x0081082	End 0 x0081089f 0 x008108af 0 x008108af 0 x008108af 0 x008108df	Add
Alt Edit Module System View 1 im Contents System Generation Component Library Nos II Processor Bridges and Adapters Hemories and Memory Control Peripherals Deploy and Performance Display FPGA Peripherals Microcontroller Peripherals Microcostroller Peripherals Microcontroller Peripherals Micr	Target Device I Use V V V	Connec	Exit Hel d_1s10.sopc (D:tu tix * Module Name seven_seg_ s1 reconfig_rec s1 stram s1 systid confro_slav pli s1 confo_slav	P Clock Ser Clock Ser Clock Ser Clock Ser Sys_c sdran	Prev Nex ttings ttings ttings ttings ttings ttings	dard_Xenomai_ dard_Xenomai_ Source External pl.c0 bl.c	enerate	MM 50,0,50,0 50,0,0 50,0,0 1,0 1,0 1,0 1,0 1,0 1,0 1,0 1,0 1,) Hz Base 0x0081089 0x0081082 0x0081082 0x0081082	End 0 0x0081089f 0 0x008108af 0 0x01fffff 8 0x0081082f 0 0x008108df	Add
Alt Edit Module System View 1 im Contents System Generation Component Library Nos II Processor Pridges and Adapters Interface Protocols Legacy Components Memories and Memory Control Perpiperals Debug and Performance Display FPGA Peripherals Microcontroller Peripherals Microcontroller Peripherals Microcontroller Peripherals Microcostroller Periphe	Fools Nios Target Device I Use V V V	Connec	Exit Hel d_1s10.sopc (D:tr tix * Module Name Seven_seg_ s1 reconfig_rec s1 stan stan stan s1 stan stan control_slav pli s1 control_slav	P Clock Ser Clock Ser Clk sys_c sdran pio pio puest_pio	Prev Nes renomal_v3istan tings b b clk out Description PIO (Parallel I/O) Avalon Memory Ma System ID Peripher Avalon Memory Ma PLL Avalon Memory Ma PL Avalon Memory Ma Avalon Memory Ma PL Avalon Memory Ma PL Avalon Memory Ma PL Avalon Memory Ma PL Avalon Memory Ma Avalon Memory Ma PL Avalon Memory Ma PL Avalon Memory Ma Avalon Memory Ma PL Avalon Memory Ma Avalon Mem	dard Xenomai dard Xenomai Source External pl.c0	enerate	MM 50,0 50,0 50,0 80,0 50,0 50,0 50,0 50,0) Base 0x0081089 0x0081089 0x0081082 0x0081082 0x0081082 0x0081082	End 0 0x0081089f 0 0x0081089f 0 0x008108af 0 0x01fffff 8 0x0081082f 0 0x0081082f 0 0x0081082f 0 0x008108bf	Add
All Edit Module System View 1 m Contents System Generation Component Library Nickles and Adapters Interface Protocols Legacy Components Hernories and Memory Control Peripherals Debug and Performance Debug and Memory Control Peripherals Microcontroller Peripherals Microcontroller Peripherals Mic	Target Device I Use V V V V	Connec	Ext Hel d_1s10.sopc (0:tu itx * Module Name State state state sysid control_slav pll state	p Clock Ser Click Sys_c sdran pio uest_pio e	Prev Nez xenomal_v3istan tings b b Character LCD Avaion Memory Ma Character LCD Avaion Memory Ma LaNB1C111 Interfate	dard Xenomai dard Xenomai Source External pl.c0 pll	enerate	MM 50,0 50,0 50,0 80,0 90,0 90,0 90,0 90,0 90,0 90,0 9	 12 Base 0×0081083 0×0081084 0×0081082 0×0081082 0×0081082 0×0081082 0×0081082 0×0081082 0×0081082 	End 0 0x0081089f 0 0x0081089f 0 0x0081088f 0 0x0081082f 0 0x0081082f 0 0x0081082f 0 0x0081082f 0 0x0081084f 0 0x0081084f	Add
All Edit Module System View 1 em Contents System Generation Component Library • Nios Il Processor Fridges and Adapters Fritertace Protocols • Legacy Components • Debug and Memory Control Peripherals • Debug and Memory Control • Debug and Memory Control • Deplay • PFGA Peripherals • Microcontroller Peripherals	Target Device I Use V V V V	Connec	Ext Hel d_1s10.sopc (0:tu tv Module Name Stan stan stan stan sysid control_slav pli stan control_slav pli stan	e e	Prev Nez xenomal_v3istan tings b b ck out Description PIO (Paralel I/O) Avaion Memory Ma System ID Peripher Avaion Memory Ma System ID Peripher Avaion Memory Ma Character LCD Avaion Memory Ma LAN9(C111) Interfa LAN9(C111) Interfa LAN9(C111) Interfa	t Card Xenomai dard Xenomai Source External pli.e0 oli.e0 oped Slave oped Slave	enerate ag.0_v3.0\std_1 ag.0_v3.0\std_1 ag.0_v3.0\std_1 ag.0_v3.0\std_1 ag.0_v3.0\std_1 a	MM 50,0 50,0 50,0 70 80 80 80 80 80 80 80 80 80 80 80 80 80	12 12 1	End 0 0x0081089f 0 0x0081089f 0 0x008108af 0 0x01fffff 8 0x0081082f 0 0x008108df 0 0x008108bf 0 0x008108bf	Add
Alt Edit Module System View 1 m Contents System Generation Component Library • Nios II Processor Bridges and Adapters • Interace Protocols • Legacy Components • Memories and Memory Control • Perpherals • Display • PFOA Peripherals • Display • PFOA Peripherals • Display • PFO (Parallel I/O) • Multprocessor Coordinatic • PL • USB • Video and Image Processing	era SOPC f fools Nios Target Device I Use V V V V V V V	Connec	Exit Hell d_1s10.sopc (D:tr d_1s10.sopc (D:tr tx tx Module Name st	p Clock Se clk sys_c sdran pio pio tuest_pio	Prev Nev Nev trings tings The second sec	t Card Xenomai dard Xenomai dard Xenomai dard Xenomai dard Xenomai dard Pl.c0 External pl.c0 Dl.	enerate	MH 50,4,500 50,7 50,7 50,7 50,7 50,7 50,7 50,7) Hz Base 0x0081089 0x0081089 0x0081080 0x0081080 0x0081080 0x0081080 0x0081080 0x0081080 0x0081080 0x0081080 0x0081080	End 0 0x0081089f 0 0x008108af 0 0x008108af 0 0x008108df 0 0x008108df 0 0x008108df 0 0x008108df 0 0x008108df 0 0x008108df 0 0x008108df	Add
Alt Edit Module System View I em Contents System Generation Component Library • Nios II Processor • Display and Adapters • Interface Protocols • Legacy Components • Display • PFOA Peripherals • Microcontroller Peripherals	Target Device I Use V V V V V V Remov	Connec	Ext Hel d_1s10.sopc (D:tr tix Module Name Stan Stan Sysid control_slav pli st Control_slav pli st control_slav pli st control_slav st control_slav pli st control_slav contro	P Clock Ser Clock Ser Sdram pio puest_pio	Prov Nex Avalon Memory Ma System ID Peripher Avalon Memory Ma LANGT (SE-223 Seri Avalon Memory Ma LANGT (SE-223 Seri Avalon Memory Ma LANGT (SE-223 Seri Avalon Memory Ma Z Address	t Card Xenomai dard Xenomai dard Xenomai dard Xenomai dard Source External plice olice oli	enerate ag.0_v3.0\std_1 Clock sys_clk sys_clk sys_clk clk sys_clk clk sys_clk e sys_clk e sys_clk Fitter: D	MM 50,(, 50,0 50,0 RQ RQ RQ RQ	4z → → → → → → → → → → → → →	End 0 0x0081089f 0 0x0081089f 0 0x008108af 0 0x01fffff 8 0x008108df 0 0x008108bf 0 0x008108bf 0 0x008108ff 0 0x008108ff	Add
Alt Edit Module System View m Contents System Generation Component Library Networks and Adapters Interface Protocols Idegacy Components Idemories and Memory Control Peripherals Memories and Memory Control Peripherals Memories and Memory Control Peripherals Microcontroller Periphera	Target Device I Use V V V V Remov	Connec	Ext Hel d_1s10.sopc (D:tr itx Module Name Stan Stan Stan Sysid control_slav pli st Control_slav pli st Control_slav pli st Control_slav pli st Control_slav pli st Control_slav pli st Control_slav pli st Control_slav pli st Control_slav pli st Control_slav control_s	e e programmi Undefined	Prov Nex trings trings things the second	t Card Xenomai Source External pl.c0 pl.	enerate	MM 50,4 50 / FG 50 / FG 60 / F) Hz Base 0x0081083 0x0081084 0x0081082 0x0081085 0x0081085 0x0081085 0x0081086	End 0 0x008108af 0 0x008108af 0 0x01fffff 8 0x008108af 0 0x008108af 0 0x008108bf 0 0x008108bf 0 0x008108bf	Add

Figures 8: Creation of new peripherals in the SoPC system

The main points to respect are:

- Peripheral name.
- IRQ attributions.
- Memory mapping for each peripheral.

It is very important to respect these rules in order to use the Xenomai port for NIOS II. All IRQ numbers must be different from 0 (Linux auto detection).

Peripheral Type	Peripheral Name	IRQ Number	Used by
32-bit Timer	hrtimer	1 *	Xenomai
64-bit Timer	hrclock	2 *	Xenomai
32-bit Timer	sys_clk_timer	3 *	Linux

Figure 9: IRQ attribution to the timers in the SoPC system

*: the IRQ number is not important according to the IRQ priority (just one priority in the NIOS II processor).

2. Memory mapping

The SoPC memory mapping must have no memory mapping overlapping.

	Target	Clock Setting	IS		
🖳 Component Library	Device Feelby Obethy				
🔲 🔍 🔍 Nios Il Processor	Device Family: Stratix	Nomo	Course		Add
Bridges and Adapters	<u>1</u>	Addres	s Map	e	Remov
-Interface Protocols					
Legacy Components		cpu.instruction_master	cpu.data_master		*
Memories and Memory Contre	pli.s1		0x008108c0 - 0x008108df		
Peripherals	cpu.jtag_debug_module	0x00810000 - 0x008107f	f 0x00810000 - 0x008107ff		17
Debug and Performance	ext_ram_pus.avaion_slave			lase	End
	ext_tiash.st	0x00000000 - 0x007ffff	r 0x0000000 - 0x007ffff		
FPGA Peripherals	ext_ram.s1	0x02000000 - 0x020ffff	r 0x02000000 - 0x020fffff		
Microcontroller Periphera	unurnip_ram_64_kbytes.s1	0x02100000 - 0x0210fff	T 0x02100000 - 0x0210ffff	IRQ	0 1
Interval Timer	sys_cik_timer.s1		0x00810800 - 0x0081081F	0x00810000	0x008107
PIO (Parallel I/O)	jtag_uart.avalur_itag_slave		0x00810820 - 0x00810827		
Multiprocessor Coordinat	uarti.si		0x00810840 - 0x00810851		
● ··PLL	hutten nic of		0x00810900 - 0x00810931		
∎-USB	led nic of		0x00810830 - 0x00810831		
			0x00810880 - 0x00810881	0x0000000	0x007fff:
	seven_seg_plu.si		0x00810890 - 0x00810891		
	recornig_request_pio.sr	0-01000000 - 0-0166664	6 0x01000000 - 0x01666666	0x0200000	0x020fff
	suramsi eveid control, eleve	0x01000000 - 0x011111	0*00910929 - 0*00910926		
	lod display control slave		0x00810828 - 0x00810821	0x02100000	0x0210ff
	lep91o111_0_stave	0-0000000 - 0-0000666	6 0x00810800 - 0x00810801		
4	uert 0 e1	0x00800000 - 0x0080111	0x00800000 - 0x00801111	0x00810860	0x008108
	htimer e1		0x00810820 - 0x00810811	0x00810900	0x008109:
	nrumer.s1		0x00810860 - 0x00810871		,
ew Edit Add					
Warning: onchip ram 64 kb					
Warping reconfig request					
Info: art flach: Elech memory		Cle	ISE		
Into. exc_nash. Hashmenory					

Figure 10: Memory mapping for the SoPC system (example)

3. NIOS II processor configuration

The NIOS II processor is configured at least in its *standard* version:

		mostretoce	ooor opu	
MegaCore'	os II Processo	r		About
Parameter				
	aches and Memory Interfaces	Advanced Features	MMU and MPU Settings	1TAG Debug Module Custom Instructi
Core Nios II	caches and Hemory Incontaces	Havancear cataros	Minio dina mino socialitas	
Select a Nice II cor	e.			
	○Nios II/e	● Nios II/s	○Nios II/f	1
Nios II Selector Guide Family: Stratix f _{system:} 50,0 MHz cpuid: 0	RISC 32-bit	RISC 32-bit Instruction Cache Branch Prediction Hardware Multiply Hardware Divide	RISC 32-bit Instruction Cache Branch Prediction Hardware Multiply Hardware Divide Barrel Shifter Data Cache Dynamic Branch Pred	liction
Performance at 50,0	MHz Up to 8 DMIPS	Up to 32 DMIPS	Up to 57 DMIPS	
Logic Usage	600-700 LEs	1200-1400 LEs	1400-1800 LEs	
Memory Usage	Two M4Ks (or equiv.)	Two M4Ks + cache	Three M4Ks + cache	
Hardware Multiply:	DSP Block	Hardware Divide	i.	
Reset Vector:	Memory Law and			
	ext_flash		JuJu	J×0000000
Exception vector: N	nemory: sdram		00×	×01000020
Only include the MM	luden using an analytica au		N.41.1	
Fast TLB Miss Excep	tion Vector: Memory:	stem triat explicitly supports all M	Offset: 0x0	

Figure 11: NIOS II processor configuration in its standard version

The instruction and data caches are enabled:

	Nios Il Processor - cpu 🔴	000
File Edit f	Nios II Processor	
Com; Bridg G-Interf G-Lega Mem G-Perip G-C G-	Parameter Settings Core Nios II Caches and Memory Interfaces Advanced Features MMU and MFU Settings JTAG Debug Module Custom Instructions Caches and Memory Interfaces Instruction Master Data Master Data Master Data Master Instruction Cache: Keytes Enable Bursts (Burst Size: 32 bytes) Help Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction master port(s). Number of ports Include tightly coupled instruction ports Include tig	Add Remove
()) Info: ex		
	Cancel < Back Next > Finish	-

Figure 12: Data and instruction cache configuration

MMU or MPU circuits are disabled (new functionalities appeared with the Quartus II version 8).

In consequence, you have to use the no-MMU Linux version (μ Clinux for NIOS II) with the NIOS II processor with or without Xenomai enabled...

	Nios II Processor	About Documentation
Parameter		
Settings		
Core Nios II Advanced E	Caches and Memory Interfaces Advanced Features	MMU and MPU Settings > JTAG Debug Module > Custom Instructions
	caures	
	cpu_resetrequest and cpu_resettaken signals	
These s You mu	signals appear on the top-level SOPC Builder system. ist manually connect these signals to logic external to the SOPC Builder s	system.
0		
couid ci	ontrol register value:	
Excention	Checking	
	Instruction (aways present with wiwo and wPo)	
	exception information (always present with Middl and MEU) :	
		Canada (Reada) Elizida
		Cancel Cancel Kext > Finish
		Cancel Cancel Next > Finish
	Nios II Proces	Cancel Cancel Next > Finish
	Nios II Processor	Cancel Cancel Next > Finist
Negeter.	Nios II Processor	Cancel < Back Next > Finist ssor - cpu About Occumentation
Megecore Parameter Settinger	Nios II Processor	Cancel < Back Next > Finish ssor - cpu [About] Documentation
Regecter Megecter Parameter Settings II	Nios II Proces Nios II Processor Caches and Memory Interfaces Advanced Features	Cancel & Back Next > Finist ssor - cpu About Documentation
Parameter Settings Core Nios II	Nios II Proces Nios II Processor Caches and Memory Interfaces Advanced Features IPU Settings	Cancel Cancel Next > Finish ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Magacon Parameter Settings Core Nios II -MMU and M	Nios II Proces Nios II Processor Caches and Memory Interfaces Advanced Features RU Settings	Cancel Cancel Next > Finist ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Arrow Core Nios II May Core Nios II MMU and M MMU Process II	Nios II Process Nios II Processor Caches and Memory Interfaces Advanced Features PU Settings O(PID) Bits: 10 Bits	Cancel & Back Next > Finist ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Parameter Settings Core Nios II -MMU and M Process II	Nios II Processor Caches and Memory Interfaces Advanced Features PU Settings (PID) Bits: 10 Bits	Cancel Cancel About Next > Finist ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Parameter Settings Core Nios II MMU and M Process II	Nios II Processor Nios II Processor Caches and Memory Interfaces Advanced Features PU Settings O(PID) Bits: 10 Bits Confidence France France France France France	Cancel & Back Next > Finist assor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Parameter Settings Core Nos II MMU and M Process II TLB Entrie	Nios Il Processor Nios II Processor Caches and Memory Interfaces Advanced Features PU Settings >(PID) Bits: 10 Bits ====================================	Cancel Cancel About Finish ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Parameter Settings Core Nos II 	Nios II Processor Caches and Memory Interfaces Advanced Features IPU Settings (PID) Bits: 10 Bits 128 Entries ssociativity: 16 Ways	Cancel & Back Next > Finist ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Parameter Settings Core Nios II 	Nios II Processor Caches and Memory Interfaces Advanced Features (PID) Bits: 10 Bits 128 Entries ssociativity: 16 Ways B Entries: 6 Entries	Cancel & Back Next > Finist ssor - cpu About Documentation MMU and MPU Settings JTAG Debug Module Custom Instructions
Parameter Settings Core Nios II 	Nios II Processor Nios II Processor Caches and Memory Interfaces Advanced Features (PID) Bits: 0 Bits Secondarivity: 128 Entries Secondarivity: 18 Ways B Entries: 6 Entries Entries: 6 Entries	Cancel < Back
Parameter Settings Core Nios II 	Nios Il Processor Nios II Processor Caches and Memory Interfaces Advanced Features PU Settings O (PID) Bits: 10 Eits Si 128 Entries Sissociativity: 16 Ways B Entries Entries: 4 Entries	Cancel < Back
Parameter Settings Core Nios II 	Nios Il Processor Nios II Processor Caches and Memory Interfaces Advanced Features PU Settings 2 (PID) Bits: 10 Bits 128 Entries ssociativity: 128 Entries Entries: 4 Entries Entries: 4 Entries	Cancel < Back
Parameter Settings Core Nios II 	Nios II Processor Nios II Processor Caches and Memory Interfaces Advanced Features (128 Entries ssociativity: 128 Entries ssociativity: 16 Ways B Entries Entries: 4 Entries Entries: 4 Entries Entries: 4 Entries	Cancel < Back
Parameter Settings Core Nios II 	Nios II Process Nios II Processor Caches and Memory Interfaces Advanced Features (120 Settings (120 Settings (120 Entries ssociativity: 10 Bits 128 Entries ssociativity: 16 Ways B Entries Entries: 4 Entr	Cancel < Back

Cancel < Back Next > Finish

📐 Warnin <u> </u>Warnin 🕕 Info: **e**) Enable the JTAG (level 1) for debugging:

1	0		Nios II Process	sor - cpu		0	0
idit t n Corr	MegaCore [®] Nio:	s II Processor			Abo	ut Documentation	
Com	Parameter Settings					-	0 al
⊷ ⊜ \ Brida	Core Nios II	thes and Memory Interfaces	Advanced Features	MMU and MPU Settings	TAG Debug Module	Custom Instructions	Add
Interf	= ITAG Dobug Medula	ches and Memory Incontaces	Havancear catares	Mino and Miro Settings			
Lega	STAO Debug Module						
Memo	Select a debugging I	level:	1	101 10	10		
Perip	O No Debugger	Level 1	O Level 2	CLevel 3	OLevel 4		
er-C er-F er-N er-N er-N		Download Software Software Breakpoints	Download Software Software Breakpoints 2 Hardware Breakpoints 2 Data Triggers	Download Software Software Breakpoints 2 Hardware Breakpoints 2 Data Triggers Instruction Trace	Download Software Software Breakpoints 4 Hardware Breakpoints 4 Data Triggers Instruction Trace Data Trace On-Chip Trace Off-Chip Trace	6	810'
USB	No LEs	300-400 LEs	800-900 LEs	2400-2700 LEs	3100-3700 LEs		
Videc	No M4Ks	Two M4Ks	Two M4Ks	Four M4Ks	Four M4Ks	7	7ff:
	Include debugreq a These signals app You must manually Break Vector Memory: cpu	and debugack signals ear on the top-level SOPC Builder y connect these signals to logic ex	system. ternal to the SOPC Builder sy /set:	ystem.	22)	1 8 8	10f 810: 810:
_	-Advanced Debug S	Settinas					
v	OCLOBCHID Trace:	00 Evenes					
		26 Frames					
/arnin	Misutometacolly ge	enerate internal 2X clock signal H	<u>elp</u>				
/arnin	Advanced debug lice	enses can be purchased from FS2	2. www.fs2.com				
fo: e)							

Figure 14: JTAG (level 1) configuration

You don't use the custom instructions:

-	1		Nios II Pro	ocessor - cpu		(000
File Edit I							
System Corr	MegaCore	Nios II Processor				About Documentation	
🛄 Com	Parameter						
- • N	Cove Mine T		Advanced Freeburgs		TAC Debut Mar		Add
± Bridg	Core Nios I.	Caches and Memory Internaces	Auvanceu reacures	/ MMO and MPO Settings	JTAG DEbug Mot		Remove
	Bitswap		Name	Clock Cycles	N Port	Opcode Extension	
	Endian Conv	verter					
🖻 Perip	Floating Poir	nt Hardware					
€-E	Interrupt Ve	ctor					
							<u>^</u>
+ 							
							I 8107f
±-N							
.∎-USB							
⊡Vide¢							7ffff
							Offff
							10444
							IOIII
							81087
							81093 -
							•
New							
Antoneia		Add Import		Remove Edit	Move Up	Move Down	
A Warnin							
A vvarnin							
U Into: e							
					[c;		

Figure 15: Custom instruction configuration

4. sys_clk_timer timer

IMPORTANT SOPC DESIGN RULE FOR XENOMAI:

When you instantiate your peripherals in your SoPC system with the *SOPC Builder* tool, the peripherals appear in the *.ptf* file in the order they have been created.

When you create the *nios2.h* file from your *.ptf* file (see 4.2), the used parser (Perl script) searches the first Altera timer and uses it as a Linux tick timer.

You must create first the *sys_clk_timer* timer in the SoPC system and then the other timers after.

If you have not done it, erase all Altera timers in your SoPC system (*SOPC Builder*), save and create again first the *sys_clk_timer* timer!

The *sys_clk_timer* timer is used by Linux as a tick timer. Its configuration with the *SoPC Builder* tool is:

- 32-bit timer.
- Timeout period: 10 ms.
- Preset: custom. Writable period, readable snapshot, Start/Stop control bits.

Edit Module	e - Altera SO	2C Builder - std_1s10.sopc* (D:tmp\design_xenomai_v3\standard_Xenomai_q9.0	_v3.0\std_1s10.sopc)		
e Ealt Module System View IC	DOIS INIOSI	interval limer - sys_cik_umer	•		
ystem Contents System Generation	Target	Interval Timer			
Nios II Processor Bridges and Adapters Interface Protocols Legacy Components Memories and Memory Control Peripherals	Device F	Parameter Settings	MHz 50,0 50,0 50.0	* R	Add
Debug and Performance	Use	Period: 10 ms	Base	End	Tags
Display FPGA Peripherals G-Microcontroller Peripherals G-Microcontroller Veripherals G-0 (Parallel I/O)		Timer counter size	0x02100000 0x00810860 0x00810900 0x00810800	0x0210ffff 0x0081087f 0x0081093f 0x0081081f	*
⊕-Multiprocessor Coordinatic		Hardware options	0x00810820	0x00810827	
PLL USB Video and Image Processing		Presets: Custom	₽ 0x00810840	0x0081085f	
		Registers	0x00810830	0x0081083f	
		 ✓ Writable period ✓ Readable snapshot 		0x0081088f	
4 · · · · · ·		Start/Stop control bits			
	•	Coutput signals	0x008108a0	0x008108af	•
New	Remove	Timeout pulse (1 clock wide) System reset on timeout (Watchdog)	it		
Karning: onchip_ram_64_kbytes:	This memor				
Warning: reconfig_request_pio: P Info: ext_flash: Flash memory capac	NO inputs ar city: 8,0 MB				
		Cancel	ish		
	L				

Figure 16: sys_clk_timer Linux timer configuration

5. hrtimer timer

The *hrtimer* timer is used by Xenomai as a high-precision clock event source. Its configuration with the *SoPC Builder* tool is:

- Timer: 32 bits.
- Timeout period: 1 µs.
- Preset : custom. Writable period, readable snapshot, Start/Stop control bits.

Edit Module System View To	ools Nios I 🚇	Interval Timer - hrtimer			
Component Library	Target Device F	Interval Timer About Documentation arameter	MHz		Add
Bridges and Adapters Interface Protocols Legacy Components Memories and Memory Control Perioherals		Timeout period	50,0 50,0 50.0	*	Remove
Debug and Performance	Use	Period: 1 us	Base	End	Tags
🖻 Display			0x02100000	0x0210ffff	
		Timer counter size	₫ 0x00810860	0x0081087f	
Microcontroller Peripherals		Counter Size: 32 with bits	0x00810900	0x0081093f	
Interval Timer Plo (Parallelulo)			0x00810800	0x0081081f	
PIO (Parallel I/O)		Hardware options	-		
multiprocessor Coordinatic			0x00810820	0x00810827	
		Presets: Custom			
			0x00810840	0x0081085f	_
ervideo and image Processing		-Registers	1		
			0x00810830	0x00810831	
		Writable period	000010000	0-00010004	
	57	Readable spapshot	0X00810880	0x00810881	
			0-0-00210220	0-00010004	
		Start/Stop control bits	0x00010070	0x00810891	
			0~008108>0	0v008108sf	
	< <u>-</u>	- Output signals	UXUUUUUU	CAUCCICCAL	
	Davis	Timeout pulse (1 clock wide)			
	Kemove	Custom venet en times et (0/stabiles)	III		
		System reset on timeout (watchdog)			
vvarning: onchip_ram_64_kbytes:	: This memor				
Warning: reconfig_request_pio : P	PIO inputs ar				
Info: ext_flash: Flash memory capa	icity: 8,0 MB				
	-				
		Cancel	ish		

Figure 17: hrtimer Xenomai timer configuration

6. hrclock timer

The *hrclock* timer is used by Xenomai as a freerunning counter for precise time stamping purpose, in the snapshot mode. Its configuration with the *SoPC Builder* tool is:

- 64-bit timer.
- Timeout period: 1 μ s. The timer functionality is not used by Xenomai.
- Preset: custom. Writable period, readable snapshot, Start/Stop control bits.

Edit Module System View T	ools Nios I 🔔	Interval Timer - hrclock	•		
tem Contents System Generation	Target	Interval Timer	nentation		
Component Library	Device F		MHZ		Add
-Bridges and Adapters -Interface Protocols -Legacy Components	Sett	nnecer ings	50,0 50,0 50,0	R	lemov
Memories and Memory Control Deripherele	E I B	neout period			
-Pehprierais -Debug and Performance	Pe	riod: 5 clocks	Bace	End	Tone
⊡ Display	036		0x0210000	0 0x0210ffff	rago
FPGA Peripherals		ner counter size	0x00810860	0 0x0081087f	
-Microcontroller Peripherals	Co	ounter Size: 64 Juits	■ 0x00810900	0 0x0081093f	
Interval Timer Interval Timer PIO (Parallel I/O)		ardware options	0x00810800) 0x0081081f	
Multiprocessor Coordinatic			■ 0x00810820) 0x00810827	
⊎-PLL ∃-USB ∃Video and Image Processing	Pri Pri	esets: Custom	₽ 0x00810840	0 0x0081085f	
		Registers	0x00810830) 0x0081083f	
		Viritable period	₽° 0x00810880) 0x0081088f	
		Start/Stop control bits	₩ 0x00810890) 0x0081089f	
		Output signals	0x008108a() 0x008108af	
ew Edit Add	Remove	Timeout pulse (1 clock wide) System reset on timeout (Watchdog)	vit		
Warning: onchip_ram_64_kbytes Warning: reconfig_request_pio: F Info: ext_flash: Flash memory capa	This memor PIO inputs ar city: 8,0 MB				
		Canr	cel Finish		

Figure 18: hrclock Xenomai timer configuration

4. SOFTWARE CONFIGURATION: A STEP BY STEP GUIDE

4.1. Altera tool installation under Linux

It is possible to use the Altera tools under Linux. In this way, we just need one machine under Linux for both HW and SW development.

The document [5] deeply explains how to do this installation. The installation procedure has been validated under Fedora 10 to Fedora 12.

We have used in this guide the version 9.0 of the *Quartus II* tools:

```
$ cd
$ wget ftp://ftp.altera.com/outgoing/release/90 quartus linux.tar
$ wget ftp://ftp.altera.com/outgoing/release/90 nios2eds linux.tar
$ wget ftp://ftp.altera.com/outgoing/release/90 modelsim ae linux.tar
$ tar -xvf 90 nios2eds linux.tar
$ cd nios2eds
# ./install
$ cd
$ tar -xvf 90 modelsim ae linux.tar
$ cd modelsim ae
# ./install
$ cd
$ tar -xvf 90 quartus linux.tar
$ cd quartus
# ./install
$ cd
```

All the Altera software has been installed under the /opt/altera9.0 directory.

```
Create the n2sdk script that you put in your ~/bin directory:

!/bin/bash

# Run this for a Nios II SDK bash shell

export LM_LICENSE_FILE=1700@localhost

SOPC_KIT_NIOS2=/opt/altera9.0/nios2eds

export SOPC_KIT_NIOS2

SOPC_BUILDER_PATH_90=/opt/altera9.0/nios2eds

export SOPC_BUILDER_PATH_90

unset GCC_EXEC_PREFIX

QUARTUS_ROOTDIR=/opt/altera9.0/quartus

export QUARTUS_ROOTDIR

export PERL5LIB=/usr/lib/perl5/5.10.0

bash --rcfile $QUARTUS_ROOTDIR/sopc_builder/bin/nios_bash
```

For using the Altera *Quartus II* and *ModelSim* tools for synthesis and simulation, you must acquire valid floating licences from Altera that you'll use with a *flexIm* server...

But you can use freely the Altera tools for programming the target board.

Install the JTAG module. In this guide, we use with the target board the USB Blaster module:

```
# mkdir /etc/jtagd
# cp /opt/altera9.0/quartus/linux/pgm_parts.txt /etc/jtagd/jtagd.pgm_parts
$ n2sdk
[NiosII EDS]$ su
Password:
# jtagd
# exit
[NiosII EDS]$ touch ~/.jtag.conf
[NiosII EDS]$ touch ~/.jtag.conf
[NiosII EDS]$ jtagconfig
1) USB-Blaster [USB 2-1.3.2]
020010DD EP1S10
```

```
Verify that the nios2-download command is ready for downloading a file into the target board:
[NiosII EDS]$ nios2-download
Using cable "USB-Blaster [USB 2-1.3.2]", device 1, instance 0x00
Pausing target processor: OK
Restarting target processor
[NiosII EDS]$
```

The Altera tools are now ready under Linux.

4.2. Linux configuration for the NIOS II processor

You have to use the NIOS processor without MMU or MPU, running a μ Clinux distribution.

```
Download the µClinux distribution for NIOS II processor [4]:
$ cd
$ wget http://www.niosftp.com/pub/uclinux/nios2-linux-20090730.tar
```

```
Install the archive file:
$ tar -xvf nios2-linux-20090730.tar
```

All the software is under the *nios2-linux* directory: \$ cd nios2-linux

Run the *checkout* script for recovering all source files and you use after the *update* script for updating:

\$./checkout
\$./update

Checkout the kernel baseline from the linux-2.6 git repository, according to the commit number mentioned for the target release, in the ksrc/nios2/patches/README file:

```
$ cd
$ cd nios2-linux/linux-2.6
$ git checkout -b ipipe d01303a1035a39e445007c7522d89ad985c4153c
```

```
Install the gcc crosscompiler for the NIOS II processor:
```

```
$ wget http://www.niosftp.com/pub/gnutools/nios2gcc-20080203.tar.bz2
# tar jxf nios2gcc-20080203.tar.bz2 -C /
```

Adjust your PATH variable in your *profile* file (~/.bash_profile): PATH=/opt/nios2/bin:\$PATH export PATH

Verify that the gcc crosscompiler for NIOS II is ready:

```
$ nios2-linux-gcc -v
Reading specs from /opt/nios2/lib/gcc/nios2-linux-uclibc/3.4.6/specs
Configured with: /root/buildroot/toolchain_build_nios2/gcc-
3.4.6/configure --prefix=/opt/nios2 --build=i386-pc-linux-gnu
--host=i386-pc-linux-gnu --target=nios2-linux-uclibc --enable-
languages=c,c++ --disable-__cxa_atexit --enable-target-optspace
--with-gnu-ld --disable-shared --disable-nls --enable-threads
--enable-multilib
Thread model: posix
gcc version 3.4.6
```

We suppose now that $\frac{\int U Clinux_dist}{\int u Clinux_dist}$ variable is the directory containing the μ Clinux source files, in our case *nios2-linux/uClinux-dist* directory.

Configure µClinux for the NIOS II processor:

\$ cd \$uClinux_dist
\$ make menuconfig

In the *menuconfig* screens, verify that the following options are enabled:

```
Vendor/Product Selection --->
    --- Select the Vendor you wish to target
        Vendor (Altera) --->
    --- Select the Product you wish to target
        Altera Products (nios2) --->
Kernel/Library/Defaults Selection --->
        --- Kernel is linux-2.6.x
        Libc Version (None) --->
[*] Default all settings (lose changes)
[] Customize Kernel Settings
[] Customize Vendor/User Settings
[] Update Default Vendor Settings
```

Create now the *nios2.h* file that is the link between the HW SoPC system and the μ Clinux software via the *.ptf* file of your design:

\$ make vendor hwselect SYSPTF=/path_to_your_design/your_design.ptf

RUNNING hwselect --- Please select which CPU you wish to build the kernel against: (1) cpu - Class: altera nios2 Type: s Version: 7.080900 Selection: 1 --- Please select a device to execute kernel from: (1) ext flash Class: altera avalon cfi flash Size: 8388608 bytes (2) onchip ram 64 kbytes Class: altera avalon onchip memory2 Size: 65536 bytes (3) ext ram Class: altera nios dev kit stratix edition sram2 Size: 1048576 bytes (4) sdram Class: altera avalon new sdram controller Size: 16777216 bytes Selection: 4 --- Summary using PTF: /home/kadionik/design xenomai/std 1s10.ptf CPU: cpu Program memory to execute from: sdram

You may configure μ Clinux for using the UART serial line as a Linux console instead of the JTAG UART emulation:

Compile now the Linux kernel:

\$ make

You can download the *zImage* file into the target board with the JTAG module: \$ n2sdk [NiosII EDS]\$ nios2-download -g images/zImage

Use the *minicom* tool for having access to the target board serial line: You can see the Linux traces: \$ minicom Uncompressing Linux... Ok, booting the kernel.

Linux version 2.6.30 (kadionik@linux01) (gcc version 3.4.6) #2 PREEMPT Fri Jan 0 uClinux/Nios II Built 1 zonelists in Zone order, mobility grouping off. Total pages: 4064 Kernel command line: NR IRQS:32 PID hash table entries: 64 (order: 6, 256 bytes) Dentry cache hash table entries: 2048 (order: 1, 8192 bytes) Inode-cache hash table entries: 1024 (order: 0, 4096 bytes) Memory available: 13604k/2492k RAM, 0k/0k ROM (1667k kernel code, 824k data) Calibrating delay loop... 24.26 BogoMIPS (lpj=121344) Mount-cache hash table entries: 512 net namespace: 264 bytes NET: Registered protocol family 16 init_BSP(): registering device resources bio: create slab <bio-0> at 0
NET: Registered protocol family 2 IP route cache hash table entries: 1024 (order: 0, 4096 bytes) TCP established hash table entries: 512 (order: 0, 4096 bytes) TCP bind hash table entries: 512 (order: -1, 2048 bytes) TCP: Hash tables configured (established 512 bind 512) TCP reno registered NET: Registered protocol family 1 io scheduler noop registered io scheduler deadline registered (default) ttyS0 at MMIO 0x810840 (irq = 5) is a Altera UART console [ttyS0] enabled ttyS1 at MMIO 0x8108e0 (irq = 8) is a Altera UART smc91x.c: v1.1, sep 22 2004 by Nicolas Pitre <nico@cam.org> eth0: SMC91C11xFD (rev 1) at 80800300 IRQ 7 [nowait] eth0: Invalid ethernet MAC address. Please set using ifconfig dm9000 Ethernet Driver, V1.31 TCP cubic registered NET: Registered protocol family 17 RPC: Registered udp transport module. RPC: Registered tcp transport module. Freeing unused kernel memory: 596k freed (0x11da000 - 0x126e000) Shell invoked to run file: /etc/rc Command: hostname uClinux Command: mount -t proc proc /proc -o noexec, nosuid, nodev Command: mount -t sysfs sysfs /sys -o noexec,nosuid,nodev Command: mount -t devpts devpts /dev/pts -o noexec, nosuid Command: mount -t usbfs none /proc/bus/usb mount: mounting none on /proc/bus/usb failed: No such file or directory Command: mkdir /var/tmp Command: mkdir /var/log Command: mkdir /var/run Command: mkdir /var/lock Command: mkdir /var/empty Command: ifconfig lo 127.0.0.1 Command: route add -net 127.0.0.0 netmask 255.0.0.0 lo Command: cat /etc/motd Welcome to || - || - ||_ | | | || |_|

For further information check: http://www.uclinux.org/

```
Execution Finished, Exiting
Sash command shell (version 1.1.1)
/>
```

4.3. Xenomai configuration for the NIOS II processor

```
Download the latest Xenomai version from the git server:
$ cd
$ git clone git://xenomai.org/xenomai-head.git
```

```
For the latest stable version (2.5.2):
    wget http://download.gna.org/xenomai/stable/xenomai-
2.5.2.tar.bz2
    tar -xvjf xenomai-2.5.2.tar.bz2
```

We suppose now that the *\$xenomai_root* variable is the directory containing the Xenomai source files.

Apply the *ipipe* patch for the NIOS II processor on the Linux kernel source files:

Compile the Xenomai utilities in order to integrate them into the romfs directory: \$./configure -host=nios2-linux \$ make install DESTDIR=\$uClinux dist/romfs

You may suppress all the Xenomai documentation in the *romfs* directory: \$\rm -rf \$uClinux_dist/romfs/usr/xenomai/share/doc \$\rm -rf \$uClinux_dist/romfs/usr/xenomai/share/man

Recompile the Linux kernel for including Xenomai support:

```
$ cd $uClinux_dist
$ make
```

Download the *zImage* file into the target board with the JTAG module: \$ n2sdk [NiosII EDS]\$ nios2-download -g images/zImage

Use the *minicom* tool for having access to the target board serial line: You can see the Linux traces: \$ minicom Uncompressing Linux... Ok, booting the kernel. Linux version 2.6.30 (kadionik@linux01) (gcc version 3.4.6) #18 PREEMPT Tue Mar0 Built 1 zonelists in Zone order, mobility grouping off. Total pages: 4064 Kernel command line: NR IRQS:32 PID hash table entries: 64 (order: 6, 256 bytes) I-pipe 1.1-00: pipeline enabled. Dentry cache hash table entries: 2048 (order: 1, 8192 bytes) Inode-cache hash table entries: 1024 (order: 0, 4096 bytes) Memory available: 11572k/4525k RAM, 0k/0k ROM (1931k kernel code, 2593k data) Calibrating delay loop... 24.06 BogoMIPS (lpj=120320) Mount-cache hash table entries: 512 net namespace: 264 bytes NET: Registered protocol family 16 init BSP(): registering device resources bio: create slab <bio-0> at 0 NET: Registered protocol family 2 IP route cache hash table entries: 1024 (order: 0, 4096 bytes) TCP established hash table entries: 512 (order: 0, 4096 bytes) TCP bind hash table entries: 512 (order: -1, 2048 bytes) TCP: Hash tables configured (established 512 bind 512) TCP reno registered NET: Registered protocol family 1 I-pipe: Domain Xenomai registered. Xenomai: hal/nios2 started. Xenomai: scheduling class idle registered. Xenomai: scheduling class rt registered. Xenomai: real-time nucleus v2.5.2 (Souls Of Distortion) loaded. Xenomai: starting native API services. Xenomai: starting POSIX services. Xenomai: starting RTDM services. io scheduler noop registered io scheduler deadline registered (default) ttyS0 at MMIO 0x810840 (irq = 5) is a Altera UART console [ttyS0] enabled ttyS1 at MMIO 0x8108e0 (irq = 8) is a Altera UART smc91x.c: v1.1, sep 22 2004 by Nicolas Pitre <nico@cam.org> eth0: SMC91C11xFD (rev 1) at 80800300 IRQ 7 [nowait] eth0: Invalid ethernet MAC address. Please set using ifconfig dm9000 Ethernet Driver, V1.31 TCP cubic registered NET: Registered protocol family 17 RPC: Registered udp transport module. RPC: Registered tcp transport module. Freeing unused kernel memory: 2276k freed (0x1232000 - 0x146a000) Shell invoked to run file: /etc/rc Command: hostname uClinux Command: mount -t proc proc /proc -o noexec, nosuid, nodev Command: mount -t sysfs sysfs /sys -o noexec, nosuid, nodev Command: mount -t devpts devpts /dev/pts -o noexec, nosuid Command: mount -t usbfs none /proc/bus/usb mount: mounting none on /proc/bus/usb failed: No such file or directory Command: mkdir /var/tmp Command: mkdir /var/log Command: mkdir /var/run Command: mkdir /var/lock Command: mkdir /var/empty Command: ifconfig lo 127.0.0.1 Command: route add -net 127.0.0.0 netmask 255.0.0.0 lo Command: cat /etc/motd Welcome to

```
_\___|_||_| ||\__|\__|\_/\_/
For further information check:
http://www.uclinux.org/
Execution Finished, Exiting
Sash command shell (version 1.1.1)
/>
/> cd /usr/xenomai/bin
/usr/xenomai/bin> ./latency -t2
== Sampling period: 10000 us
== Test mode: in-kernel timer handler
== All results in microseconds
warming up...
RTT| 00:00:01 (in-kernel timer handler, 10000 us period, priority 99)
RTH|-----lat min|-----lat avg|-----lat max|-overrun|----lat best|---lat worst
         73.080| 83.223| 90.020|
                                                 0 |
                                                        73.080|
                                                                      90.020
RTD|
                      55.164|
                                 104.840|
                                                 0 |
                                                                     104.840
RTD|
          1.820|
                                                         1.820|
                                 106.160
          3.240|
                      65.454|
                                                 0 |
                                                         1.820
                                                                     106.160
RTD|
                                                         0.920|
0.920|
RTDI
          0.920|
                      63.1671
                                  100.8001
                                                 0 |
                                                                     106.160
RTD|
          1.160|
                      65.735|
                                  103.860|
                                                 0 |
                                                                     106.160
                      62.741|
                                  105.180|
                                                                     106.160
RTD|
         -0.600|
                                                 0 |
                                                         -0.600|
                                  105.480|
                      64.406
                                                         -0.600|
                                                                     106.160
          3.520|
                                                0 |
RTD|
          1.720|
                      65.379|
                                 105.100|
                                                0 |
                                                         -0.600|
                                                                     106.160
RTD
          2.280|
                      66.0601
                                 106.980|
                                                0 |
                                                         -0.600|
                                                                     106.980
RTD
RTD|
          4.900|
                      65.314|
                                 106.320|
                                                 0 |
                                                         -0.600|
                                                                     106.980
```

5. **REFERENCES**

[1] The Xenomai project. http://www.xenomai.org

[2] The µClinux project for the NIOS II processor. http://www.nioswiki.com/

[3] The QuartusforLinux page. http://www.nioswiki.com/OperatingSystems/UClinux/QuartusforLinux

[4] The InstallNios2Linux page. http://www.nioswiki.com/InstallNios2Linux

[5] Altera tools under Linux : ftp://ftp.altera.com/outgoing/release